In the Claims:

1. (currently amended) A sigma-delta modulator, comprising:

~~an~~ digital feedback signal source for providing a digital feedback signal;

a passive discrete time circuit for receiving the digital feedback signal and an input signal, the input signal comprising information and a pair of ~~one or more~~ analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time; and summing the analog feedback signal and a selected one of said pair of ~~the one or more~~ analog input currents during a second discrete time to yield a ~~one or more~~ summed signals;

a passive continuous time circuit comprising a plurality of passive resistive and capacitive elements, the continuous time circuit coupled to the discrete time circuit to filter the ~~one or more~~ summed signals using a first first-order filter containing resistive and capacitive elements serially connected to a second first order filter containing resistive and capacitive elements to form a second first order filter to generate a ~~one or more~~ filtered signals, the first-order filters comprising one or more first passive elements of the plurality of passive elements, and

a quantizer coupled to the continuous time circuit to generate the digital signal using the ~~one or more~~ filtered signals, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals.

2. (currently amended) The sigma delta modulator of Claim 1, further comprising a transconductance circuit to: receive the input signals comprising the information~~, the input signal having one or more analog input voltages;~~ and convert the ~~one or more~~ analog input voltages into ~~one or more~~ analog input currents.

3. (previously presented) The sigma-delta modulator of Claim 1, wherein the discrete time circuit converts the digital feedback signal into an analog feedback signal using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time.

4. (previously presented) The sigma-delta modulator of Claim 1, wherein:

the one or more passive elements associated with the first first order filter comprises a first capacitor; and

the one or more passive elements associated with the second first order filter comprises a second capacitor and a resistor.

5. (currently amended) A sigma-delta modulator, comprising:

a discrete time circuit for receiving a digital feedback signal and an input signal, the input signal comprising information and a pair of ~~one or more~~ analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time; and summing the analog feedback signal and a selected one of said pair of ~~the one or more~~ analog input currents during a second discrete time to yield ~~one or more~~ a summed signals;

a continuous time circuit comprising a plurality of passive elements, the continuous time circuit coupled to the discrete time circuit and operable to filter the ~~one or more~~ summed signals using a first first-order filter serially connected to a second first order filter to form a second order filter in order to generate a ~~one or more~~ filtered signals, the first-order filters comprising one or more first passive elements of the plurality of passive elements; and

a quantizer coupled to the continuous time circuit and operable to generate the digital signal using the ~~one or more~~ filtered signals, the digital signal comprising the information; wherein:

the discrete time circuit comprises a reference capacitor, the reference capacitor associated with a reference capacitance;

the ~~one or more~~ passive elements associated with the first first order filter comprises a first capacitor, the first capacitor associated with a first capacitance; and

the ratio between the first capacitance and the reference capacitance is substantially greater than one.

6. (previously presented) The sigma-delta modulator of Claim 1, wherein:

the one or more passive elements associated with the second first order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

7. (currently amended) The sigma-delta modulator of Claim 1, wherein the quantizer comprises a comparator to generate the digital signal using the ~~one or more~~ filtered signals by:

amplifying the ~~one or more~~ filtered signals; and

comparing the ~~one or more~~ filtered signals to ~~each~~ another filtered signal to quantize an error associated with the input signal and the digital signal.

8. (previously presented) The sigma-delta modulator of Claim 1, wherein the output of the quantizer is coupled to the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal.

9. (currently amended) A method for converting an input signal into a digital signal, comprising the steps of:

providing a passive discrete time circuit;

at said passive discrete time circuit (a) receiving a digital feedback signal and ~~an~~ a pair of input signals ~~at said a passive discrete time circuit~~, the input signals comprising information and ~~one or more~~ analog input currents; (b) converting the digital feedback signal into an analog feedback signal during a first discrete time; and (c) summing the analog feedback signal and a selected one of the ~~one or more~~ analog input currents during a second discrete time to yield a ~~one or more~~ summed signals;

providing a passive continuous time circuit;

at said passive continuous time circuit (a) filtering the ~~one or more~~ summed signals at a continuous time circuit in order to generate a ~~one or more~~ filtered signals, the continuous time circuit comprising a first passive first-order filter and a second passive ~~second~~ first order filter, the first first-order filter comprising one or more first passive resistive and capacitive elements of the plurality of passive elements, the second first order filter comprising one or more second passive resistive and capacitive elements of the plurality of passive elements; and (b) generating the digital signal using the ~~one or more~~ filtered signals, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals.

10. (currently amended) The method of Claim 9, further comprising:

receiving at a transconductance circuit the input signal comprising the information, the input signal having said pair of ~~one or more~~ analog input voltages; and

converting the ~~one or more~~ analog input voltages into the one or more analog input currents.

11. (previously presented) The method of Claim 9, wherein converting the digital feedback signal into an analog feedback signal during the first discrete time further comprises using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time.

12. (previously presented) The method of Claim 9, wherein:

the one or more first passive elements associated with the first first order filter comprises a first capacitor; and

the one or more second passive elements associated with the second first order filter comprises a second capacitor and a resistor.

13. (previously presented) A method for converting an input signal into a digital signal, comprising the steps of:

providing a discrete time circuit;

at said discrete time circuit (a) receiving a digital feedback signal and an input signal at a discrete time circuit, the input signal comprising information and one or more analog input currents; (b) converting the digital feedback signal into an analog feedback signal during a first discrete time; and (c) summing the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals;

providing a continuous time circuit;

at said continuous time circuit (a) filtering the one or more summed signals at a continuous time circuit in order to generate one or more filtered signals, the continuous time circuit comprising a first first-order passive filter and a second first order passive filter, the first first-order filter comprising one or more first passive elements of the plurality of passive elements, the second first order passive filter comprising one or more second passive elements of the plurality of passive elements; and (b) generating the digital signal using the one or more filtered signals, the digital signal comprising the information;

wherein: the discrete time circuit comprises a reference capacitor;

the one or more first passive elements associated with the first first order filter comprises a first capacitor; and

the ratio between the first capacitor and the reference capacitor is substantially greater than one.

14. (previously presented) The method of Claim 9, wherein:

the one or more second passive elements associated with the second first order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

15. (currently amended) The method of Claim 9, wherein generating the digital signal using the one or more filtered signals further comprises:

amplifying the ~~one or more~~ filtered signals; and

comparing at a comparator the ~~one or more~~ filtered signals to another filtered signal ~~each other~~ to quantize an error associated with the input signal and the digital signal.

16. (previously presented) The method of Claim 9, wherein the output of the quantizer is coupled to the discrete time circuit to form a passive feedback loop, the passive feedback loop converting the digital signal into an analog feedback signal.

17. currently amended) A sigma-delta modulator, comprising:

means for receiving a digital feedback signal and a pair of analog ~~an~~ input signals at a discrete time circuit, the input signal comprising information and ~~one or more~~ analog input currents;

means for converting the digital feedback signal into an analog feedback signal during a first discrete time;

means for summing the analog feedback signal and a selected one of said pair of ~~the one or more~~ analog input currents during a second discrete time to yield ~~one or more~~ a summed signals;

means for filtering the ~~one or more~~ summed signals at a continuous time circuit in order to generate a ~~one or more~~ filtered signals, the continuous time circuit comprising a first passive first-order filter and a passive second passive first order filter, each filter containing both resistive and capacitive elements; and

means for generating the digital signal using the ~~one or more~~ filtered signals, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals.

18. (previously presented) A sigma-delta modulator, comprising:

a discrete time circuit to: receive a digital feedback signal and an input signal, the input signal comprising information and one or more analog input currents; convert the digital feedback signal into an analog feedback signal during a first discrete time using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time; and sum the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals, the discrete time circuit further comprising a reference capacitor, the reference capacitor associated with a reference capacitance;

a passive continuous time circuit comprising a plurality of passive elements, the continuous time circuit coupled to the discrete time circuit and filtering the one or more summed signals using a first first-order filter and a second first order filter in order to generate one or more filtered signals, the first first-order filter comprising one or more first passive elements of the plurality of passive elements, the second first order filter comprising one or more second passive elements of the plurality of passive elements, the one or more first passive elements associated with the first first order filter comprising a first capacitor, the one or more second passive elements associated with the second first order filter comprising a second capacitor and a resistor, the ratio between the first capacitance and the reference capacitance is substantially greater than one;

a quantizer coupled to the continuous time circuit and operable to generate the digital signal using the one or more filtered signals, the digital signal comprising the information; and

a transconductance circuit ~~operable to:~~ for receiving the input signal comprising the information, the input signal having one or more analog input voltages; and

converting the one or more analog input voltages into one or more analog input currents.

19. (previously presented) The sigma-delta modulator of Claim 18, wherein:

the one or more second passive elements associated with the second first order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

20. (previously presented) The sigma-delta modulator of Claim 18, wherein the quantizer comprises a comparator operable to generate the digital signal using the one or more filtered signals by:

amplifying the one or more filtered signals; and

comparing the one or more filtered signals to each other to quantize an error associated with the input signal and the digital signal, wherein the output of the comparator is coupled to the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal.